SNAP+
Data Sheet

Revision 1.06

profichip®
automation in silicon

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Liability Exclusion

We have tested the contents of this document regarding agreement with the hardware and software described. Nevertheless, there may be deviations and we do not guarantee complete agreement. The data in the document is tested periodically, however. Required corrections are included in subsequent versions. We gratefully accept suggestions for improvements.

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Preliminary

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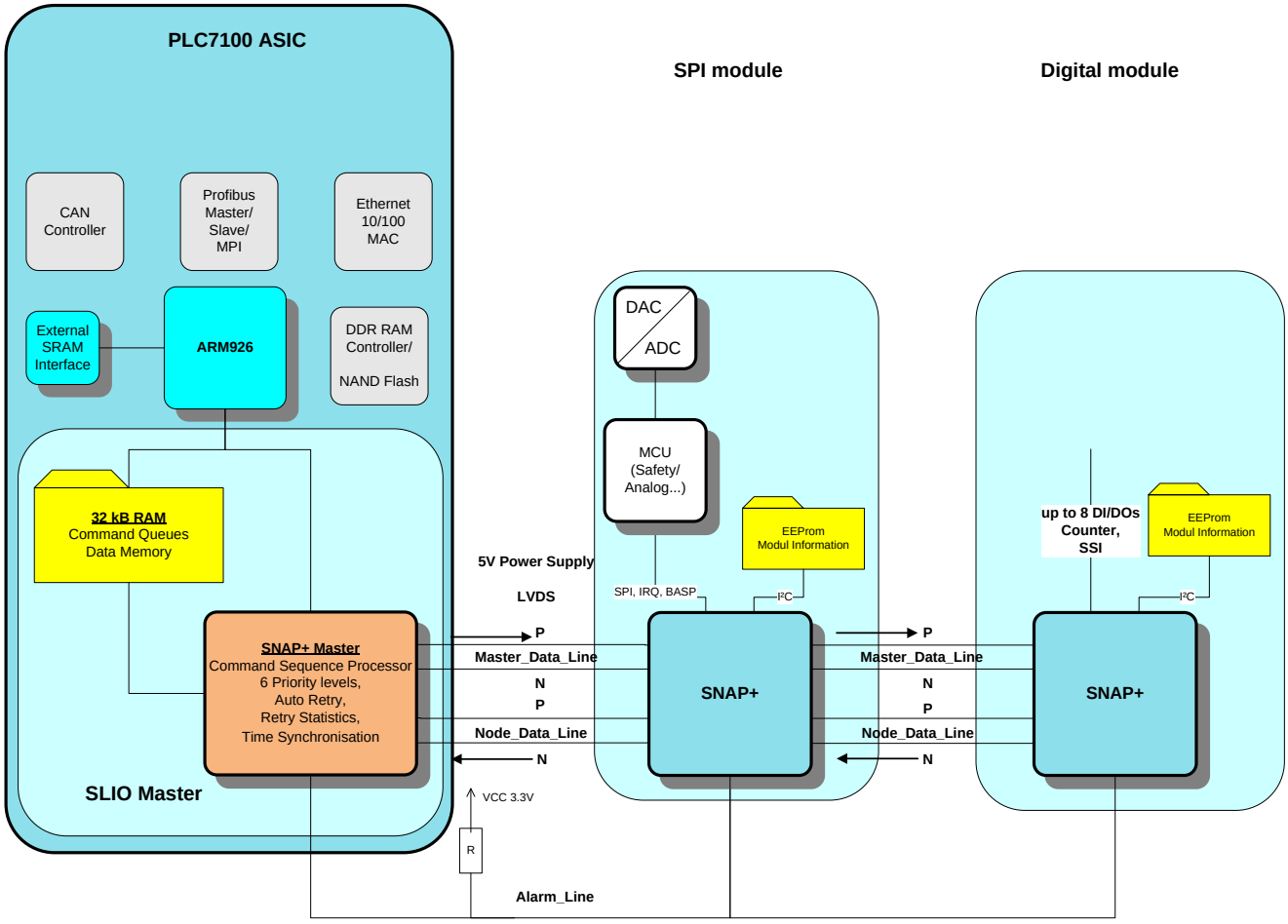
Preliminary

1 Overview

1.1 SNAP+ Typical Application



1.2 SNAP+ Features

BasicSliceBus information:

- Single master system
- Up to 64 slaves (SNAP+ modules) stations
- Asynchronous, serial data transmission with 48 MBit/s over Point to Point LVDS physic
- Additional alarm line for initialization and asynchronous event communications from SNAP+ module (slave at SliceBus) to SNAP+ Master
- Full system detection from SNAP+ Master without external information on module configuration

Error detection mechanism:

- CRC code with Hamming distance 4 for every telegram (all 3 bit errors will be detected)
- Watchdog function inside every SNAP+ module for SNAP+ Master observation
- “Auto shut down” in case of SNAP+ Master malfunction
- Retry statistic for early detection of possible transmission issues

Time-synchronisation:

- Every SNAP+ module has its own clock with 1µs resolution
- All SNAP+ module clocks are synchronized with the SNAP+ Master (accuracy <100ns)
- Option for clock synchronization from SNP+ Master to SNAP+ Master via different protocols (Profibus DP V2, Profinet, Ethercat,...)

Technological functions in SNAP+:

- Standard I/O function: 8 digital I/O or 16DI or 16DO with shift register
- Integrated digital input filter function
- Asynchronous event signaling with µs time stamping for advanced SNAP+ modules
- Two advanced counters with AB oversampling, latch, reset, output, hysteresis, comparevalue, repetitive/endless counting and additional time stamp information
- SSI function with time stamp information (speed calculations: counter difference/time)
- Pulse Width Modulation with 20ns resolution
- Frequency measurement mode
- Special digital I/O time stamp modules (ETS: Edge Time Stamp System) for input edge and output control with 1µs resolution (independent from fieldbus cycle!)

SPI interface in SNAP+ for analog I/O / safety / serial CP with external MCU:

- 2.6 MBit/s SPI interface for external microcontroller
- Up to 192 Byte for parameters, up to 16 byte In / 16 byte Out data for external microcontroller
- Alarm function and watchdog function

Performance:

- Different „Speed Grades“ for data transmission
- Multi-module telegrams for maximum efficiency:
  → Write 64 modules (8 outputs/SNAP+): 17µs
  → Read 64 modules (8 inputs/SNAP+): 32µs (with module presence check)

Mechanical and electrical specification SNAP+:

- I/O voltage: 3,3V, typ. 16mA, core voltage: 1,8V, typ. 16mA
- DI8 or DO8 modul without I/O load: typical: 5V, 32mA
- LQFP 48 package, 9x9mm², pitch 0,5mm

2 Pin Description

2.1 Pin Assignment

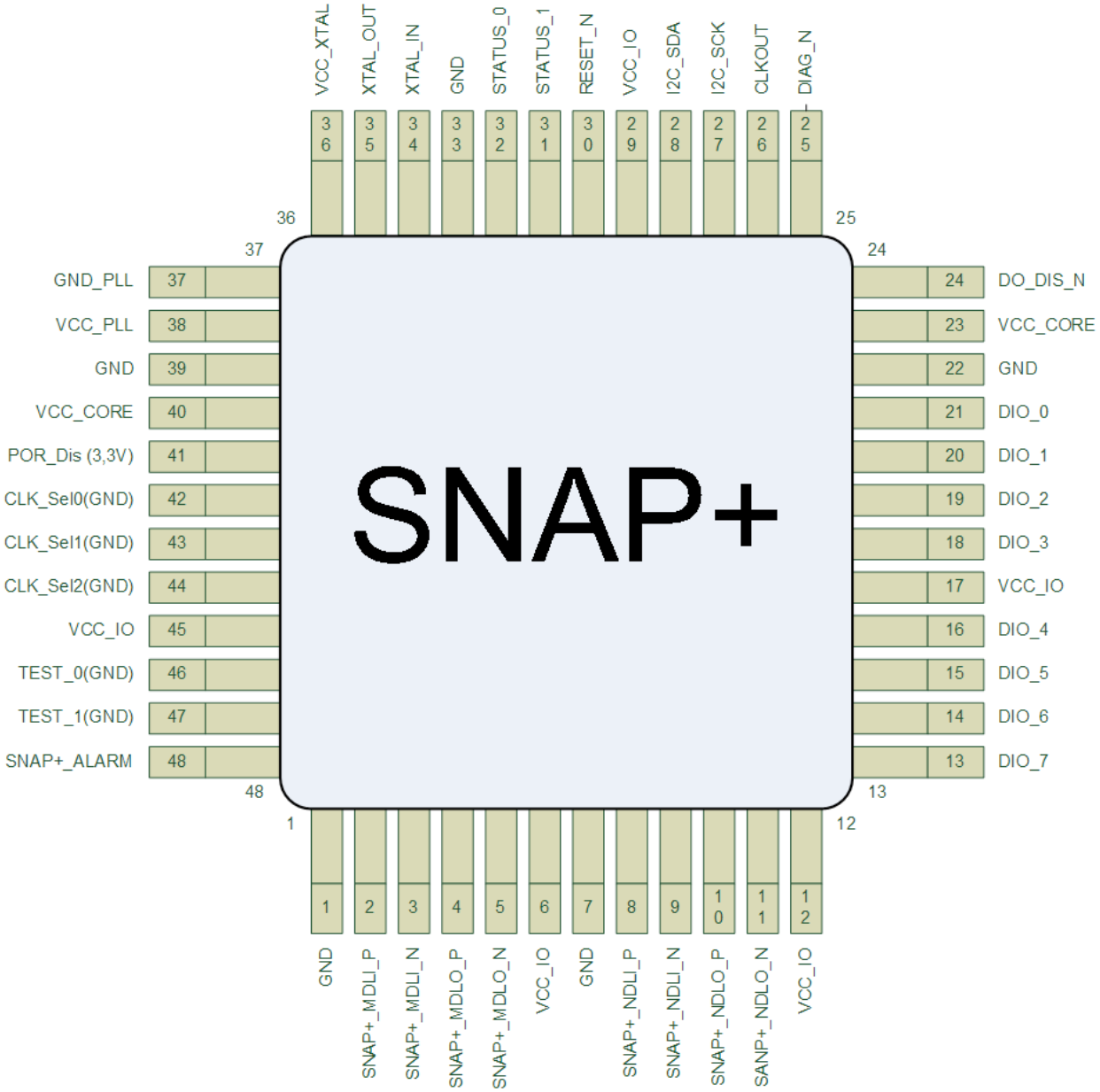
Pin	Signal	Direction	Description
1	GND		
2	SNAP+_MDLI_P	IN (LVDS)	SNAP+ bus: Master-Data-Line-IN positive (LVDS)
3	SNAP+_MDLI_N	IN (LVDS)	SNAP+ bus: Master-Data-Line-IN negative (LVDS)
4	SNAP+_MDLO_P	OUT (LVDS)	SNAP+ bus: Master-Data-Line-OUT positive (LVDS)
5	SNAP+_MDLO_N	OUT (LVDS)	SNAP+ bus: Master-Data-Line-OUT negative (LVDS)
6	VCCIO		
7	GND		
8	SNAP+_NDLI_P	IN (LVDS)	SNAP+ bus: Node-Data-Line-IN positive (LVDS)
9	SNAP+_NDLI_N	IN (LVDS)	SNAP+ bus: Node-Data-Line-IN negative (LVDS)
10	SNAP+_NDLO_P	OUT (LVDS)	SNAP+ bus: Node-Data-Line-OUT positive (LVDS)
11	SNAP+_NDLO_N	OUT (LVDS)	SNAP+ bus: Node-Data-Line-OUT negative (LVDS)
12	VCCIO		
13	DIO 7	INOUT (S)	DI / DO / Technological Function (depending on configuration)
14	DIO 6	INOUT (S)	DI / DO / Technological Function (depending on configuration)
15	DIO 5	INOUT (S)	DI / DO / Technological Function (depending on configuration)
16	DIO 4	INOUT (S)	DI / DO / Technological Function / SPI (depending on configuration)
17	VCCIO		
18	DIO 3	INOUT (S)	DI / DO / Technological Function / SPI (depending on configuration)
19	DIO 2	INOUT (S)	DI / DO / Technological Function / SPI (depending on configuration)
20	DIO 1	INOUT (S)	DI / DO / Technological Function / SPI (depending on configuration)
21	DIO 0	INOUT (S)	DI / DO / Technological Function / SPI (depending on configuration)
22	GND		
23	VCCCORE		
24	DO_DIS_N	OUT	Disable Outputs (active low)
25	DIAG_N	IN (S)	Request Diagnosis (active low)
26	CLKOUT	OUT	Clock Output (12 MHz)
27	I2C_SCK	OUT	I2C bus to EPROM: clock
28	I2C_SDA	INOUT (S)	I2C bus to EPROM: data
29	VCCIO		
30	RESET_N	IN (S)	Reset (active low)
31	STATUS 1	OUT	Status LED 1
32	STATUS 0	OUT	Status LED 0
33	GND		
34	XTALIN	IN (S)	XTAL input (24 MHz)
35	XTALOUT	OUT	XTAL output
36	VCCXTAL		
37	GNDPLL		

38	VCCPLL		
39	GND		
40	VCCCORE		
41	POR_Dis	IN	Connect to VCCIO
42	CLK_Sel0	IN	Connect to GND
43	CLK_Sel1	IN	Connect to GND
44	CLK_Sel2	IN	Connect to GND
45	VCCIO		
46	TEST_0	IN	Connect to GND
47	TEST_1	IN	Connect to GND
48	SNAP+_ALARM	OUT	SNAP+ bus: alarm line

Notes:

VCCCORE	+ 1.8 V
VCCXTAL	+ 1.8 V
VCCPLL	+ 1.8 V
VCCIO	+ 3.3 V
GND	0 V
(LVDS)	LVDS buffer
(S)	LVTTL Input buffer with Schmitt-Trigger

2.2 Symbol



3 Operational Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Core power supply	VCCCORE	-0.3 to 2.16	V
IO power supply	VCCIO	-0.3 to 4.0	V
Input voltage	V_{IN}	-0.3 to 4.0	V
DC input current	I_{IN}	20	mA
Output short circuit current	I_{OUT}	20	mA
Storage temperature	T_{STG}	-40 to +150	°C

Figure 3-1: Absolute Maximum Ratings

3.2 Thermal Characteristics

Parameter	Symbol	Value	Unit
thermal resistance junction to case	$R_{th\ JC}$	27.88	K/W
thermal resistance junction to ambient	$R_{th\ JA}$	72.25	K/W

Figure 3-2: Thermal Characteristics

3.3 Reliability Information

Parameter	Symbol	Value	Unit
Failure in Time (FIT) at 125°C (Failure in 10^9 Hours) HTOL (High Temperature Operating Live)	FIT	50.9	

3.4 Recommended Operating Conditions

Parameter	Symbol	MIN	MAX	Unit
Core power supply	VCCCORE	1.62	1.92	V
IO power supply	VCCIO	2.97	3.60	V
Input voltage	V_{IN}	0	3.63	V
Junction Temperature	T_J	-40	+125	°C

Figure 3-3: Recommended Operating Conditions

3.5 DC Characteristics of LVTTL IO cells

Parameter	Symbol	MIN	TYP	MAX	Unit
Input LOW voltage	V_{IL}			0.8	V
Input HIGH voltage	V_{IH}	2.0			
Switching threshold	V_T		1.5		V
Schmitt trigger negative going threshold voltage	V_{T-}	0.8	1.1		V
Schmitt trigger positive going threshold voltage	V_{T+}		1.6	2.0	V
Output LOW voltage	V_{OL}			0.4	V
Output HIGH voltage	V_{OH}	2.4			V
Input leakage current	I_{In}	-10	±1	+10	µA
Tri-state leakage current	I_{OZ}	-10	±1	+10	µA
Current consumption (3.3V)	I_{A33}		16	28	mA
Current consumption (1.8V)	I_{A18}		16	28	mA
Input capacitance	C_{IN}		2.2		pF
Output capacitance	C_{OUT}		2.2		pF
Bi-directional buffer capacitance	C_{BID}		2.2		pF

Figure 3-4: DC Characteristics of LVTTL IO cells

3.6 Package

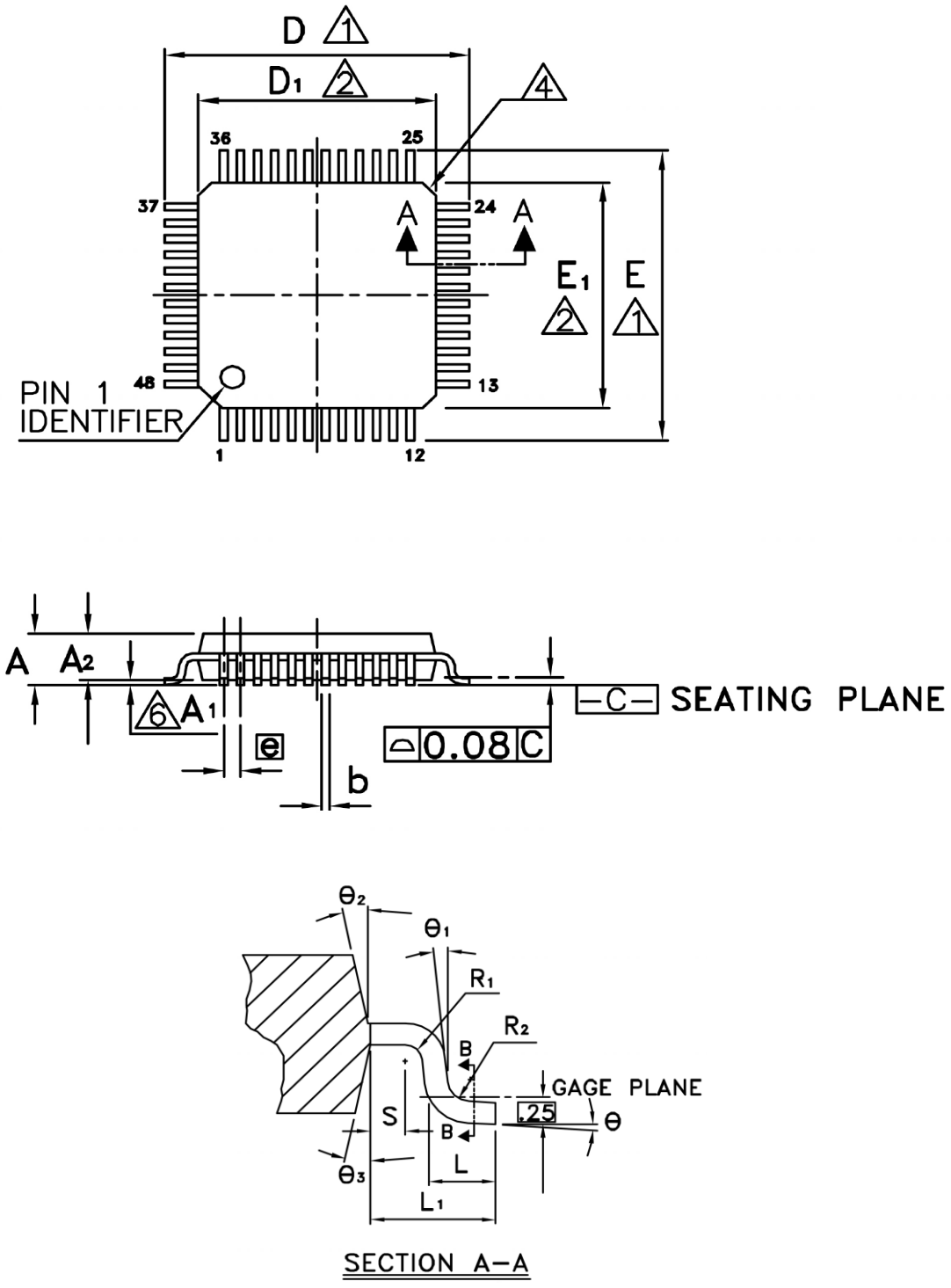


Figure 3-5: Package Drawing

Symbol	Dimensions in mm		
	MIN	NOM	MAX
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
b_1	0.17	0.20	0.23
c	0.09		0.20
c_1	0.09		0.16
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08		
R_2	0.08		0.20
S	0.20		
Θ	0°	3.5°	7°
$Θ_1$	0°		
$Θ_2$	12° TYP		
$Θ_3$	12° TYP		

Figure 3-6 : Package Dimensions and Tolerances

4 LVDS Characteristics

4.1 LVDS Schematic and Termination

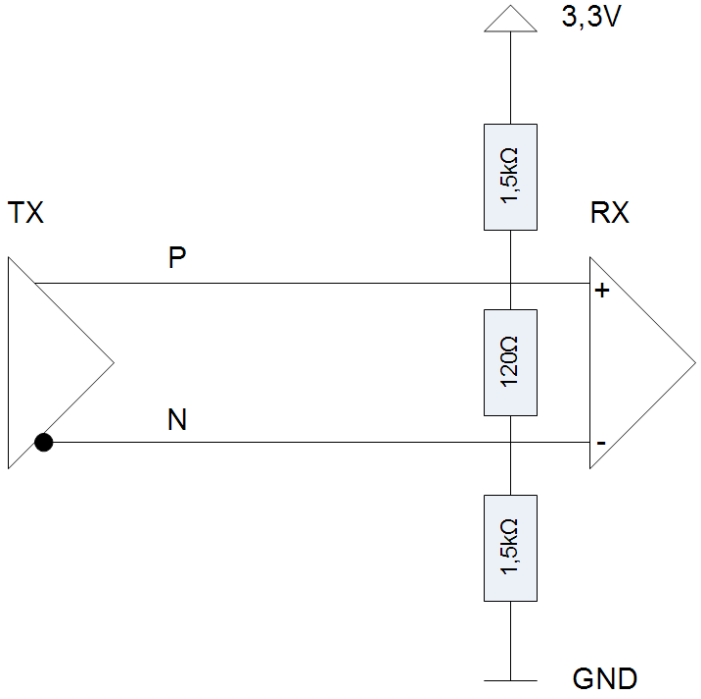


Figure 4-1: LVDS Termination

4.2 DC/AC Characteristics of LVDS IO cells

Parameter	Symbol	MIN	TYP	MAX	Unit
Differential input voltage P-N	V_{ID}	±100			mV
Input common-mode voltage	V_{IC}	$\|V_{ID}\|/2$	1.25	2.2-$\|V_{ID}\|/2$	V
LVDS driver output current	I_o		±3		mA

Figure 4-2: Characteristics of LVDS IO cells

4.3 LVDS Signal Characteristics

CH1 Yellow: LVDS_TX_P (MasterDataLineOut_P) (with 1250mV Offset)
CH2 Purple: LVDS_TX_N (MasterDataLineOut_N) (with 1250mV Offset)
M1 Red: Differential Signal CH1-CH2
Measurement Setup: MDLO_P and MDLO_N at the output of SNAP+

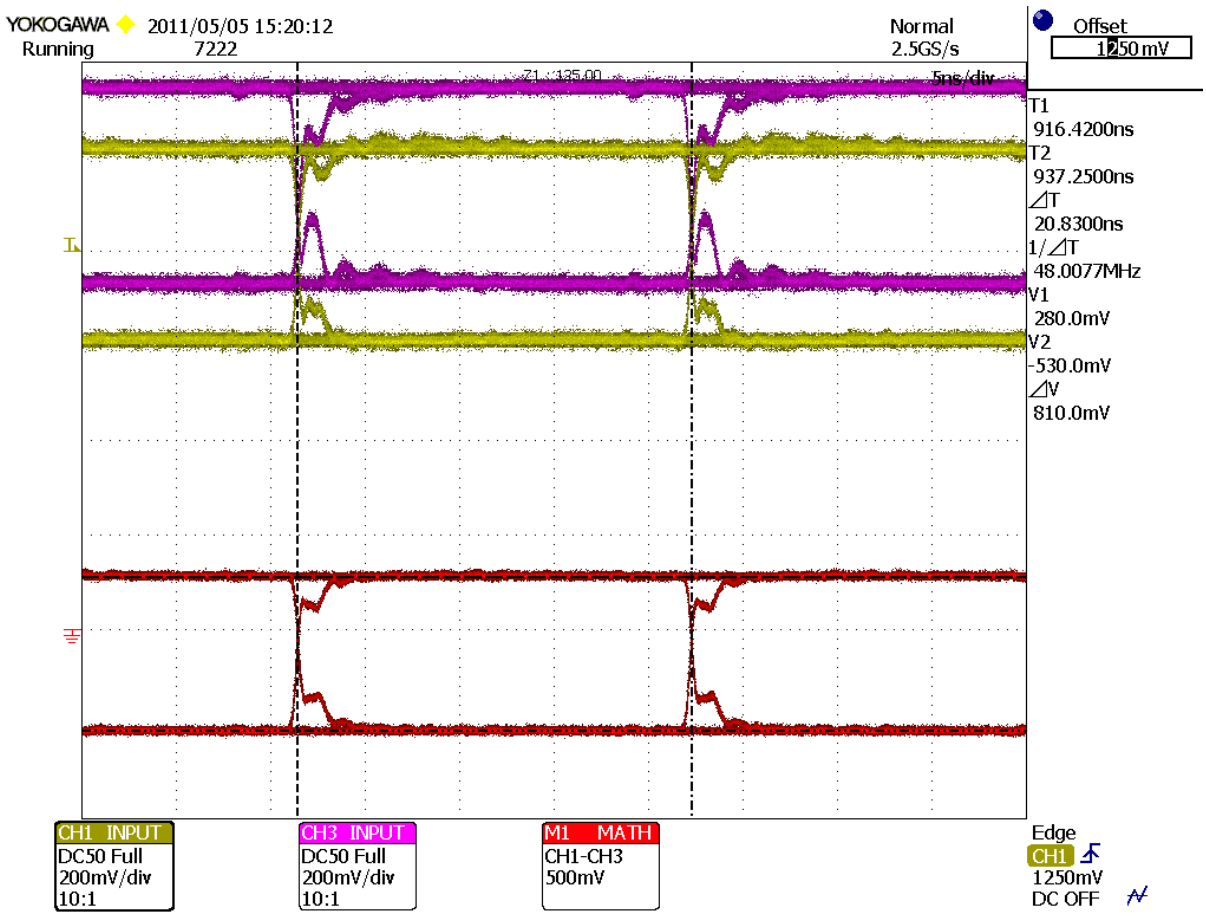


Figure 4-3: LVDS Signal

5 Layout and Schematic Recommendations

5.1 Layout Example

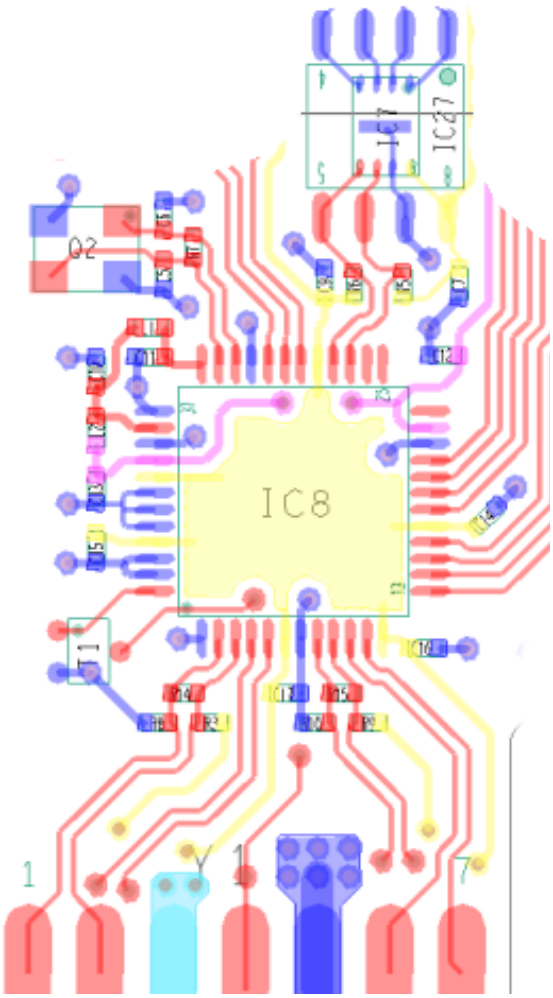


Figure 5-1: Layout Example: IC8: SNAP+, Q2 Crystal; IC27: EEPROM

5.2 Schematic Example

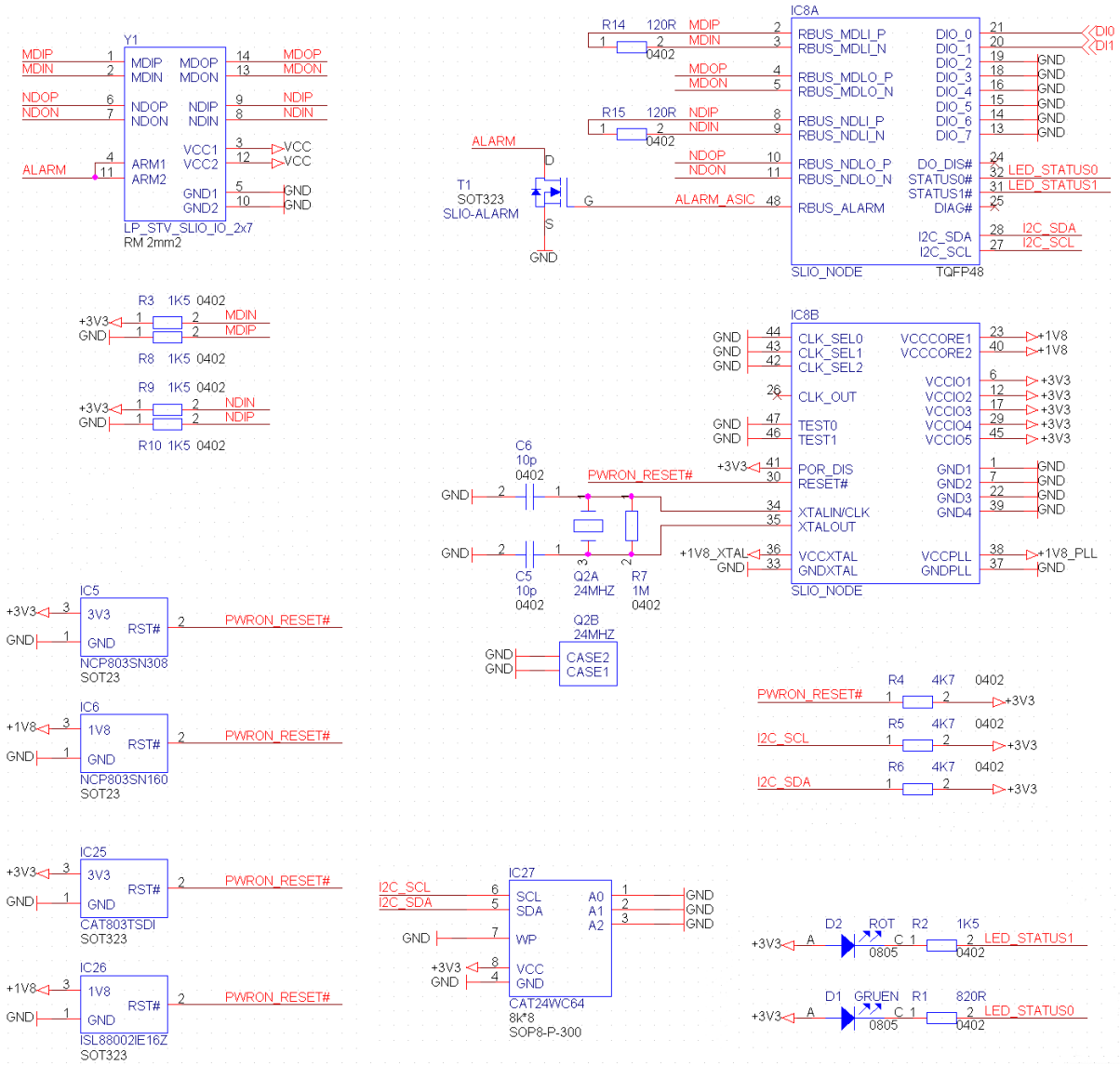
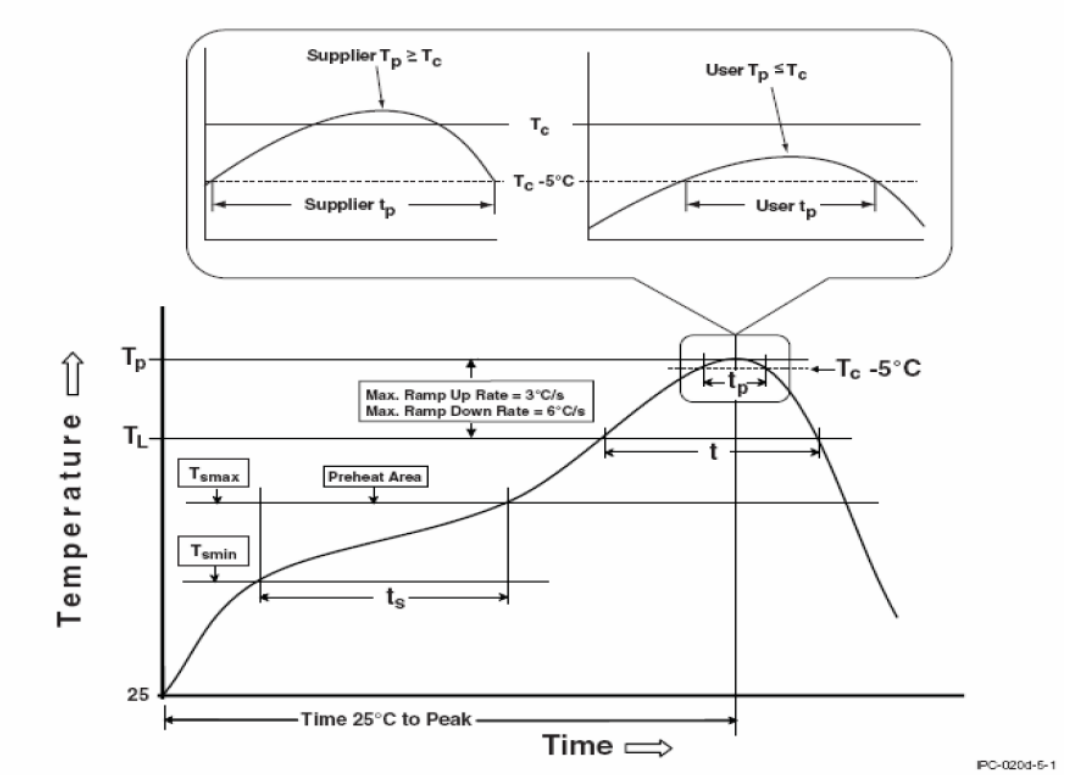


Figure 5-2: Example Schematic

6 Soldering Profile

Profichip Green Package Reflow Profile
based on IPC/JEDEC J-STD-020D



Profile Feature	Pb-Free Assembly (260°C)
Preheat and Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 150 °C 200 °C 60-120 seconds
Average ramp-up rate Time (T_{smax} to T_p)	 3 °C/second max.
Liquid temperature (T_L) Time at liquid (t_L)	217 °C 60-150 seconds
Peak package body temperature (T_p)*	260°C
Time (t_p) ** within 5 °C of the specified classification temperature (T_c)	30** seconds.
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.	

7 Order Information

Order Code:

PA007713

Delivery form:

Tray

Revision History

Version	Date	Page	Remarks
V1.00	08.03.2011		First release
V1.01	12.04.2011		Added Layout Example
V1.02	29.04.2011		Added Thermal Resistance, Changed SPI Speed Value, Added Schematic, Added LVDS Schematic, added LVDS Signals, Changed current consumption to typical
V1.03	5.05.2011		Added Soldering Profile, replaces Figure 4-3
V1.04	5.5.2011		No 32 Bit Option in Shift Register Mode, Added SNAP+ Symbol
V1.05	6.5.2011		Added Order Information
V1.06	27.5.11	17 13 6,8 9 18 10	Fixed Soldering Information (one Line to much) Added Output Driver Current Value Fixed Pins VCC XTAL and GND XTAL Added Reliability Information Added Delivery form: Tray Added max. Current Consumption

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