

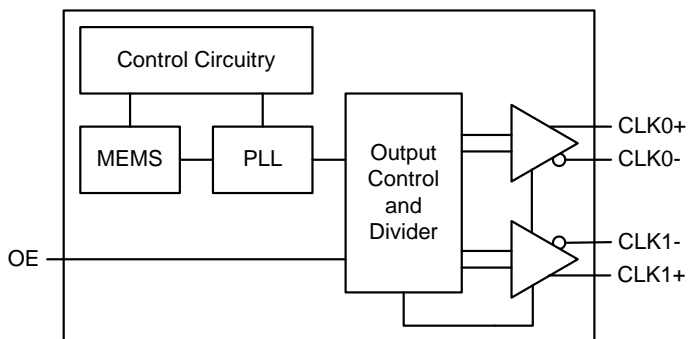


General Description

The DSC557-03 is a crystal-less, two output PCI express clock generator meeting Gen1, Gen2, and Gen3 specifications. The clock generator uses proven silicon MEMS technology to provide 100MHz* differential output clocks with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, the DSSC557-03 significantly enhances reliability and accelerates product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC557-03 has an Output Enable / Disable feature allowing it to disable the outputs when OE is low. The device is available in two different packages; a "drop-in" replacement 16 pin TSSOP or a space saving 14 pin QFN (77% less board space). Additional output formats are also available in any combination of LVPECL, LVDS, and HCSL.

Block Diagram



* Clk0+/- and Clk1+/- are 100 MHz as per PCIe standards. For other frequencies, please contact the factory.

Features

- **Meets PCIe Gen1, Gen2 & Gen3 specs.**
- **Available Output Formats:**
 - HCSL, LVPECL, or LVDS
 - HCSL/LVPECL, HCSL/LVDS, LVPECL/LVDS
- **Wide Temperature Range**
 - Ext. Industrial: -40° to 105° C
 - Industrial: -40° to 85° C
 - Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
 - 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
 - Qualified to MIL-STD-883
- **Available Footprints:**
 - 16 TSSOP
 - 14 QFN
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**

Applications

- **Communications/Networking**
 - Ethernet
 - 1G, 10GBASE-T/KR/LR/SR, and FcoE
 - Routers and Switches
 - Gateways, VoIP, Wireless AP's
 - Passive Optical Networks
- **Storage**
 - SAN, NAS, SSD, JBOD
- **Embedded Applications**
 - Industrial, Medical, and Avionics
 - Security Systems and Office Automation
 - Digital Sinage, POS and others
- **Consumer Electronics**
 - Smart TV, Bluray, STB

Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V _{DD}		2.25		3.6	V
Supply Current	I _{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current ² (Two HCSL Outputs)	I _{DD}	EN pin high – outputs are enabled R _L =50 Ω, F _{O1} =F _{O2} =100 MHz		60		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±100	ppm
					±50	
Startup Time ³	t _{SU}				5	ms
Input Logic Levels Input logic high Input logic low	V _{IH}		0.75xV _{DD}		-	V
	V _{IL}		-		0.25xV _{DD}	
Output Disable Time ⁴	t _{DA}				5	ns
Output Enable Time	t _{EN}				20	ns
Pull-Up Resistor ²		Pull-up on OE pin		40		kΩ

HCSL Outputs ⁶						
Parameter		Condition	Min.	Typ.	Max.	Unit
Output Logic Levels Output logic high Output logic low	V _{OH}	R _L =50Ω	0.725		-	V
	V _{OL}		-		0.1	
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time ⁴ Rise Time Fall Time	t _R	20% to 80% R _L =50Ω, C _L = 2pF	200		400	ps
	t _F					
Frequency	f ₀	Single Frequency	2.3	100 ⁷	460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	J _{PER}	F _{O1} =F _{O2} =100 MHz		2.5		ps _{RMS}
Jitter, Phase (Common Clock Architecture)	R _J	PCIe Gen 1.1 T _J =D _J + 14.069 x R _J (BER 10-12)		0.540		ps _{RMS}
	D _J T _J	PCIe Gen 1.1 T _J =D _J + 14.069 x R _J (BER 10-12)		0.832 8.536	41.9 ⁸ 86.0 ⁸	ps _{P-P}
	J _{RMS-CCHF}	PCIe Gen 2.1, 1.5 MHz to Nyquist		0.458	3.1 ⁸	ps _{RMS}
	J _{RMS-CCLF}	PCIe Gen 2.1, 10 kHz to 1.5 MHz		0.030	3.0 ⁸	ps _{RMS}
	J _{RMS-CC}	PCIe Gen 3.0		0.165	1.0 ⁸	ps _{RMS}
Integrated Phase Noise (Data Clock Architecture)	J _{RMS-DCHF}	PCIe Gen 2.1, 1.5 MHz to Nyquist		0.561	4.0 ⁸	ps _{RMS}
	J _{RMS-DCLF}	PCIe Gen 2.1, 10 kHz to 1.5 MHz		1.778	7.5 ⁸	ps _{RMS}
	J _{RMS-DC}	PCIe Gen 3.0		0.147	1.0 ⁸	ps _{RMS}

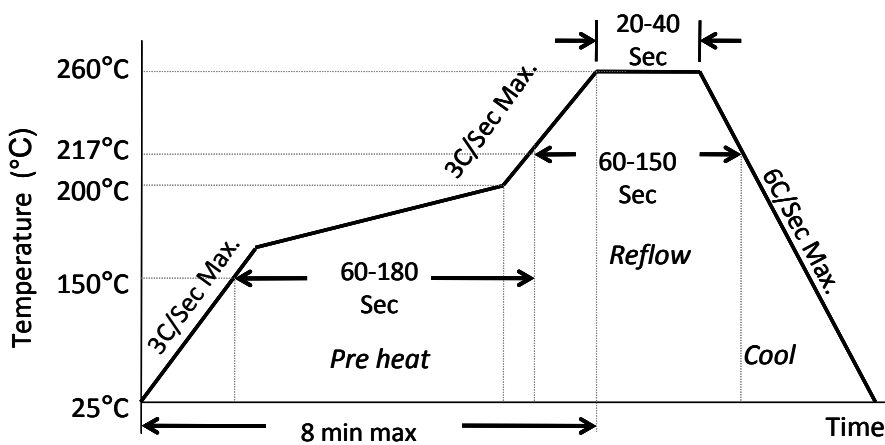
Notes:

- V_{DD} should be filtered with 0.01uf capacitor.
- Output is enabled if OE pin is floated or not connected.
- t_{SU} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
- Output Waveform and Connection Diagram define the parameters.
- Period Jitter includes crosstalk from adjacent output.
- Contact Sales@Discera.com for alternate output options (LVPECL, LVDS, LVCMOS).
- Contact Sales@Discera.com for alternate frequency options
- Jitter limits established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

Absolute Maximum Ratings

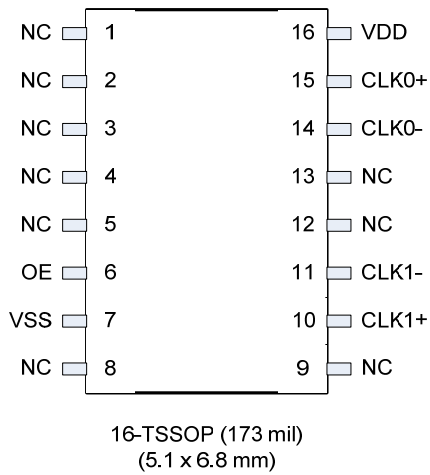
Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Solder Reflow Profile

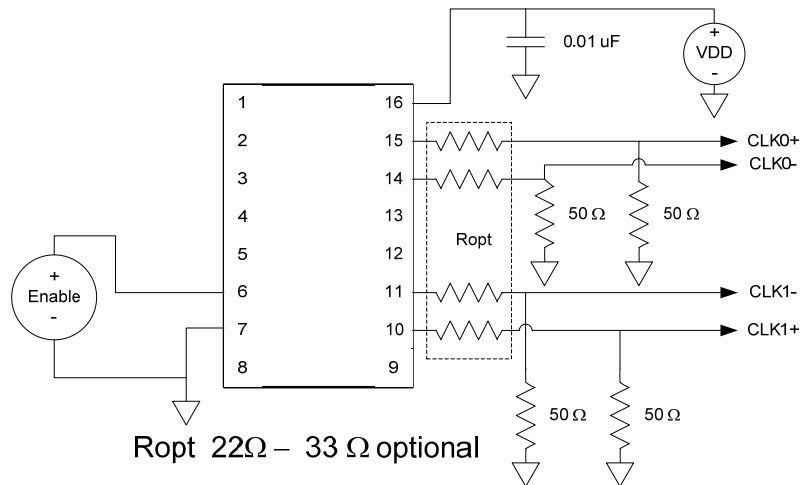


14 QFN MSL 1 @ 260°C refer to JSTD-020C 16 TSSOP MSL 3 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Pin Diagram (16 TSSOP)



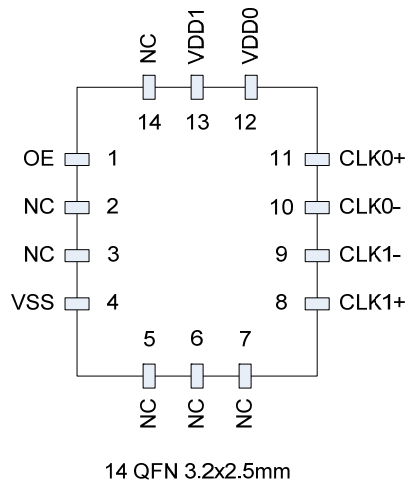
Connection Diagram (16 TSSOP Two HCSL Outputs)



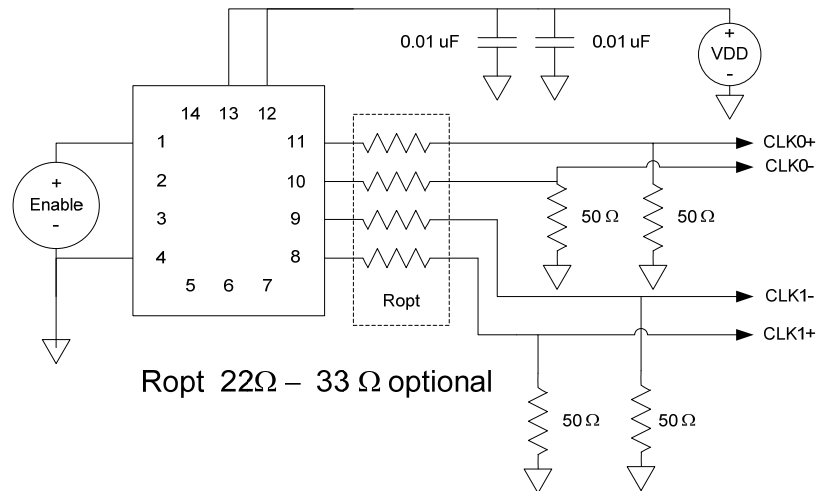
Pin Description (16 TSSOP)

Pin No.	Pin Name ⁹	Pin Type	Description
1	NC	NA	No connect
2	NC	NA	No connect
3	NC	NA	No connect
4	NC	NA	No connect
5	NC	NA	No connect
6	OE	I	Output Enable; active high
7	VSS	Power	Ground
8	NC	NA	No connect
9	NC	NA	No connect
10	CLK1+	O	True output of differential pair
11	CLK1-	O	Complement output of differential pair
12	NC	NA	No connect
13	NC	NA	No connect
14	CLK0-	O	Complement output of differential pair
15	CLK0+	O	True output of differential pair
16	VDD	Power	Power Supply

Pin Diagram (14 QFN)



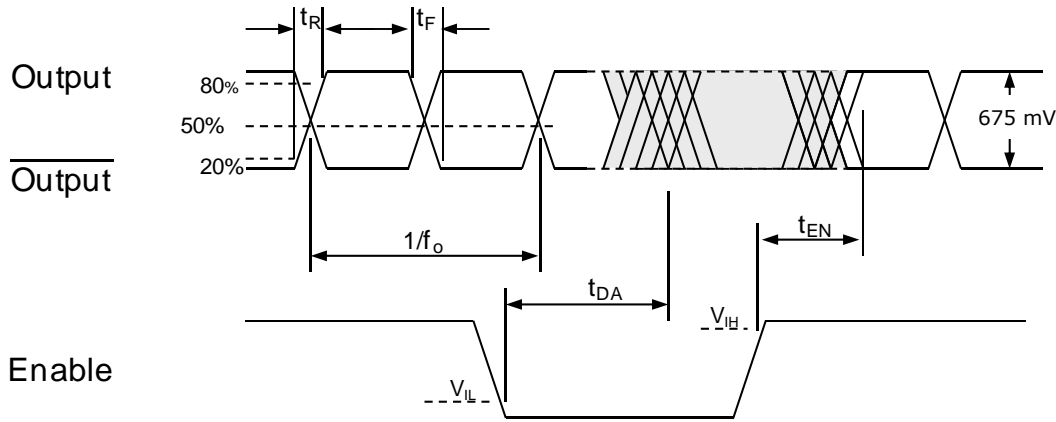
Connection Diagram (14 QFN Two HCSL Outputs)



Pin Description (14 QFN)

Pin No.	Pin Name	Pin Type	Description
1	OE	I	Output Enable; active high
2	NC	NA	Ground recommended or leave as a NC
3	NC	NA	Ground recommended or leave as a NC
4	VSS	Power	Ground
5	NC	NA	Ground recommended or leave as a NC
6	NC	NA	Ground recommended or leave as a NC
7	NC	NA	Ground recommended or leave as a NC
8	CLK1+	O	True output of differential pair
9	CLK1-	O	Complement output of differential pair
10	CLK0-	O	Complement output of differential pair
11	CLK0+	O	True output of differential pair
12	VDD1	Power	Power Supply for Core and Output 1 (CLK0+/-)
13	VDD0	Power	Power Supply for Output 0 (CLK1+/-)
14	NC	NA	Ground recommended or leave as a NC

OE Function and Output Waveform: HCSL



Ordering Information⁹

DSC557-03 4 4 F I 0 - T

CLK 1 Output Format
 1: LVCMOS
 2: LVPECL
 3: LVDS
 4: **HCSL**

CLK 0 Output Format
 1: LVCMOS
 2: LVPECL
 3: LVDS
 4: **HCSL**

- Packing
T: Tape & Reel
- Stability
0: ±100ppm
 1: ±50ppm
- Temp Range
 E: -20 to 70
I: -40 to 85
 L: -40 to 105
- Package
F: 14 QFN
 S: 16 TSSOP

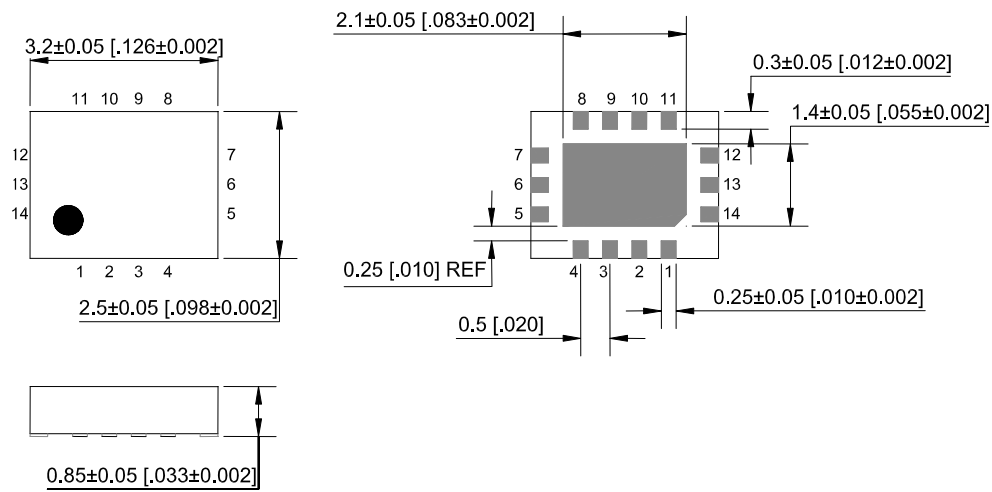
Note 9. CLK0 and CLK1 are configured at the factory to 100 MHz. (For other frequencies, contact the factory at sales@discera.com.)

Package Dimensions

F: 14 QFN, 3.2 x 2.5 mm

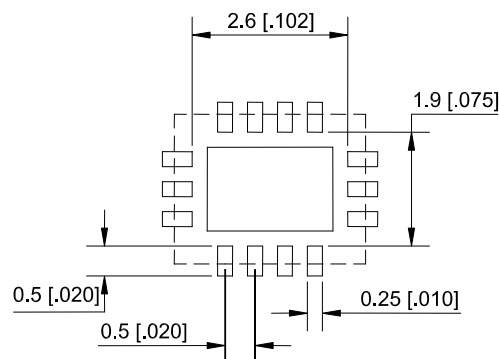
External Dimensions

units: mm[inch]

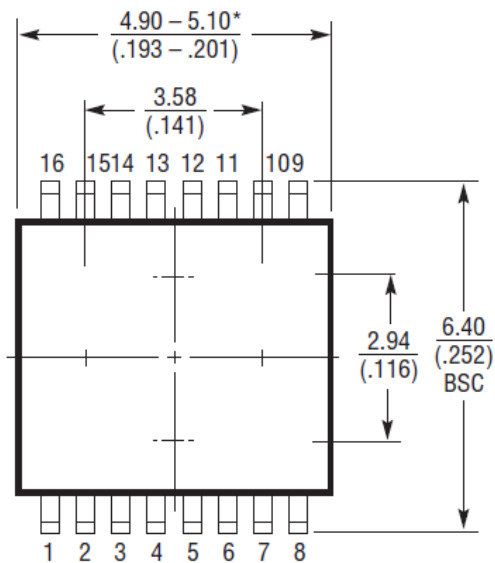
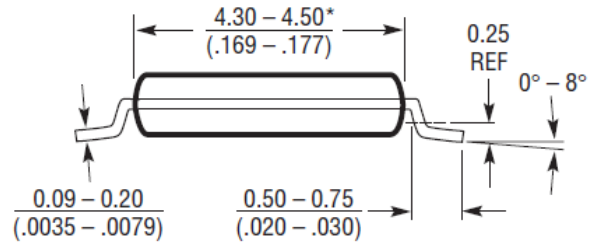
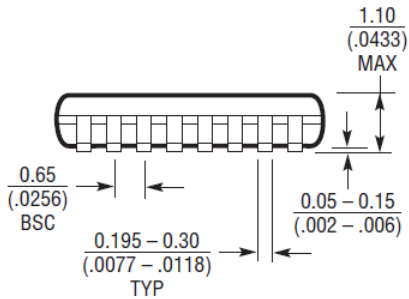


Recommended Solder Pad Layout

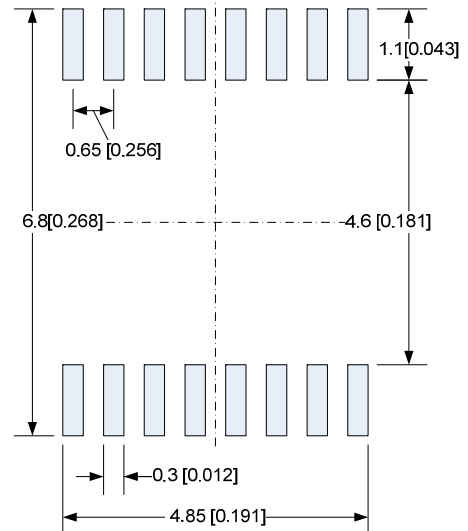
units: mm[inch]



S: 16 TSSOP (173 mil body width)



Recommended Solder Pad Layout
Units mm [in]



NOTE:

1. CONTROLLING DIMENSION: MILLIMETERS

2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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